CLAIMS

What is claimed is:

1. A computer system, comprising:

a plurality of processors coupled together between which messages can be routed;

an I/O controller coupled to one or more of said processors;

at least one I/O device coupled to an I/O controller; and

wherein each processor is capable of detecting an error in a message sent from another processor in the system and reformatting the message to indicate to other of said processors that the message contains a transmission error.

2. The computer system of claim 1 wherein each of said messages between said processors comprises multiple ticks, each tick comprising multiple bits of information, and wherein upon detecting an error has occurred in a tick, the processor alters the tick in a predetermined manner to indicate to other of said processors that the message contains an error.

3. The computer system of claim 1 wherein each of said messages between said processors comprises multiple ticks, each tick comprising multiple bits of information including error check bits, and wherein upon detecting an error has occurred in a tick, the processor alters the tick in a predetermined manner to indicate to other of said processors that the message contains an error.

4. The computer system of claim wherein 1 wherein each of said messages between said processors comprises multiple ticks, each tick comprising multiple bits of information, and wherein

upon detecting an error has occurred in a tick, the processor replaces the bits of information in the tick with a predetermined bit pattern.

5. The computer system of claim 4 wherein said predetermined bit pattern includes a known double bit error code.

6. The computer system of claim 1 wherein each of said messages between said processors comprises multiple ticks, each tick comprising data bits and error check bits, and wherein upon detecting an error has occurred in a tick, the processor replaces all of the bits in the tick with a predetermined bit pattern.

7. The computer system of claim 6 wherein said predetermined bit pattern all 1's in place of said data bits and an otherwise unused check bit code for said error check bits.

8. A processor, comprising:

a memory controller that coordinates transactions to a memory device; and

a router coupled to said memory controller and providing interfaces to one or more other processors;

wherein said router is capable of detecting a transmission error in a message received from another processor and reformatting the message to indicate that the message contains a transmission error that has already been detected.

9. The processor of claim 8 wherein said message comprises multiple sequential blocks of data, each data block comprising multiple bits of information, and wherein upon detecting that a transmission error has occurred in a data block, the router alters the block in a predetermined manner to indicate that the message contains a transmission error.

10. The processor of claim 8 wherein said message comprises multiple sequential blocks of data, each data block comprising multiple bits of information including error check bits, and wherein upon detecting that a transmission error has occurred in a data block, the router alters the data block in a predetermined manner to that the message contains a transmission error.

11. The computer system of claim wherein 8 wherein said message comprises multiple sequential blocks of data, each data block comprising multiple bits of information, and wherein upon detecting that a transmission error has occurred in a data block, the router replaces the bits of information in the data block with a predetermined bit pattern.

12. The computer system of claim 11 wherein said predetermined bit pattern includes a known double bit error code.

13. The computer system of claim 8 said message comprises multiple sequential blocks of data, each data block comprising data bits and error check bits, and wherein upon detecting that a transmission error has occurred in a data block, the router replaces the all of the bits in the data block with a predetermined bit pattern.

14. The computer system of claim 13 wherein said predetermined bit pattern includes all 1's in place of said data bits and an otherwise unused check bit code for said error check bits.

15. A method of fault isolation in a multi-processor computer system, comprising:

(a) receiving a message;

(b) detecting an error in said message;

(c) replacing the erroneous portion of said message with a predetermined bit pattern to indicate to other processors in said system that an error has occurred in said message and said error has already been detected; and

(d) transmitting the message to another processor in said system.

16. The method of claim 15 wherein said message includes a data portion and an associated error code portion and (c) includes replacing said data portion with all 1's and replacing said error code portion with an otherwise unused value.

17. The method of claim 15 further including:

(e) alerting the system that a fault has been detected in said message.

18. The method of claim 17 further including:

(f) receiving said message that has been altered in (c);

(g) determining whether said message includes said predetermined bit pattern; and

(h) if said message includes said predetermines bit pattern, not alerting the system that a fault is present in said message.

19. The method of claim 18 further including:

(i) transmitting said message with said predetermined bit pattern to another processor in said system.

20. The method of claim 15 further including:

(j) receiving said message that has been altered in (c);

(k) determining whether said message includes said predetermined bit pattern; and

(l) if said message includes said predetermines bit pattern, not alerting the system that a fault is present in said message.

21. The method of claim 20 further including:

(m) transmitting said message with said predetermined bit pattern to another processor in said system.